REMARKS

Applicants have: 1) amended no claims; 2) added no new claims; and 3) canceled no claims. As such, claims 1 – 48 are now pending. Applicants respectfully request reconsideration of the present application and consideration of the following remarks and the claims.

Claim Rejections - 35 U.S.C. § 102

"Claims 1-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Eric Swanson (U.S. Patent No. 6,751,690)."

The Office Action rejected claims 1-48 as being anticipated by Swanson. Applicants respectfully disagree. In particular, the Office Action rejected independent claims 1, 17, and 33 over Swanson asserting that "*Swanson teaches a method to design a circuit*" comprising each and every element of claim 1, claim 17, or claim 33. Applicants respectfully disagree.

For example, claim 1 reads:

1. (Original) A method to design a circuit, the method comprising:
   determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit;
   transforming a first portion of the first design to generate a second portion of a second design of the circuit;
   selectively determining at least one node in the second portion of the second design; and

determining second statistical circuit activity data for the at least one node in the second portion of the second design from the first statistical circuit activity data.

The Office Action rejected claim 1 over Swanson and it stated that "*Swanson teaches a method to design a circuit, the method comprising ...*". Applicants respectfully disagree. Swanson does not teach or suggest a method to design a circuit. As is clearly stated in Swanson, Swanson is generally concerned with "a data converter", an integrated circuit for processing data, and in particular it teaches a method and an apparatus for processing statistical data. On the other hand, the embodiment of the present invention, as claimed in claim 1, pertains to methods for designing circuits. (Please refer to the application, in particular, FIGS. 9 and 10, for various exemplary methods which may be used while "designing circuits".) Applicants respectfully request withdrawal of the rejection since the reference relied upon for the rejection is not relevant for the claimed invention.

In rejecting claim 1, the Examiner relied upon FIGS. 21-23, FIGS. 29-32, and Col. 21 line 43 to Col. 22 line 29 of Swanson for the claim limitation "determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit". Applicants respectfully disagree. Applicants submit that the cited part of Swanson does not show "first statistical circuit activity data at a plurality of nodes of ...". Furthermore, Swanson is completely silent on "determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit". Applicants respectfully request that the Examiner point out specific places, in the cited part or anywhere in Swanson, where this limitation is disclosed. It should be noted that "statistical circuit activity", as used in claim 1, includes, among other things, "the probability of signal switching at a point in the circuit, which can be used in the estimation of the power consumption of the circuit" (Paragraph [0006] lines 4-6 of the application), "a) probability information of state transition at a node; b) probability information of the node being at a state;

and c) probability information of a group of nodes being at a state" (Paragraph [0010] lines 9-10 of the application), and "the probability of signal switching at a node, the probability of a node being a given state, the probability of a correlation group being in a given state" (Paragraph [0056] lines 8-9 of the application). It should be further noted that "statistical circuit activity data", as claimed in claim 1, may be used "to calculate the power consumption at various points in the process of synthesis transformation" (Paragraph [0009] lines 9-11 of the application). Applicants respectfully submit that Swanson does not teach or suggest, either explicitly or implicitly, the element of claim 1, "determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit".

In rejecting claim 1, the Examiner further relied upon FIGS. 29-32 and Col. 28 line 35 to Col. 29 line 59 of Swanson for the limitation of "transforming a first portion of the first design to generate a second portion of a second design of the circuit". Applicants respectfully disagree. Swanson does not show "the first design" and "a second design of the circuit". Furthermore, Swanson is completely silent on "transforming a first portion of the first design to generate ...". Applicants respectfully submit that Swanson does not teach or suggest, either explicitly or implicitly, the element of claim 1, "transforming a first portion of the first design to generate a second portion of a second design of the circuit", and they respectfully request that the Examiner point out specific lines or specific parts in the figures, in the cited part or anywhere in Swanson, where this limitation is disclosed. It should be noted that "transforming [a] design of the circuit", as used in various embodiments of the present invention and as will be recognized by one of ordinary skill in the art, may include operations such as "replicating a register", "pushing a register through a logic element", "changing encoding of a finite state machine", "retiming", or "changing encoding of a group of nodes" (Paragraph [0010] lines 36-39 of the application). It should be further noted that "[d]uring the logic synthesis, the logic circuit design" may be "transformed" "(e.g., through operations such as

logic transformation, register replication, finite state machine implementation, pushing a register through a logic element, retiming)" (Paragraph [0005] lines 3-5 of the application).

Furthermore, the Examiner relied upon FIGS. 29-32 and Col. 27 line 37 to Col. 30 line 54 of Swanson for the claim limitation "selectively determining at least one node in the second portion of the second design". Applicants respectfully disagree. Applicants respectfully submit that they fail to find this claim limitation in the cited part or anywhere in Swanson, and they respectfully request the Examiner to point out specific places in Swanson where this limitation is shown.

For the claim limitation "determining second statistical circuit activity data for the at least one node in the second portion of the second design from the first statistical circuit activity data", the Examiner again relied upon FIGS. 21-23, FIGS. 29-32, Col. 21 line 43 to Col. 22 line 29, and Col. 27 line 37 to Col. 30 line 54 of Swanson. Applicants respectfully disagree. Swanson does not show "second statistical circuit activity data". Neither does it teach or suggest the claim element "determining second statistical circuit activity data for the at least one node in the second portion of the second design from the first statistical circuit activity data". Applicants respectfully request that the Examiner point out specific places in Swanson where this element of claim 1 is disclosed.

Therefore, at least for the above reasons, Applicants respectfully submit that claim 1 is patentable over Swanson since the prior art does not show each and every element of the pending claim. Furthermore, Applicants respectfully submit that the reference is not relevant for the claimed invention.

At least for the foregoing reasons, independent claims 17 and 33 are likewise patentable over Swanson, which have similar limitations as in claim 1. Since the reference relied upon for the

rejection does not show each and every aspect of the claims, the withdrawal of the rejection is respectfully requested.

The remaining claims depend on at least one of the independent claims discussed above, and therefore include at least some of the distinguishing claim limitations as discussed above. As a result, the remaining claims are also patentable. Applicants respectfully request reconsideration of these claims.

CONCLUSION

For all the above reasons, Applicants submit that the specification and claims are now in proper form, and that the claims all define patentably over the prior art. Therefore they submit that all rejections have been overcome and that all pending claims are in condition for allowance, which action they respectfully solicit. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact Jimmi Yoon at (408) 720-8300, extension 305.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due or credit any overages. If an extension is required, Applicants hereby request such extension.

Respectfully Submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Hyoungsoo "Jimmi" Yoon
Reg. No.: 57,637

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300